Docket No.: 49657-700 **PATENT** 

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Tsutomu YOSHIMURA, et al.

Serial No.:

Group Art Unit:

Filed: June 01, 2000

Examiner:

For:

A DIGITAL SYNCHRONOUS CIRCUIT FOR STABLY GENERATING OUTPUT

CLOCK SYNCHRONIZED WITH INPUT DATA

## **INFORMATION DISCLOSURE STATEMENT**

Assistant Commissioner for Patents Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Date: June 1, 2000

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION		ATTY. DOCKET NO. 49657-700		SERIAL NO.						
				APPLICANT Tsutomu YOSHIMURA, et al.						
(PTO-1449)			FILING DATI		GROUP					
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	OTHER	ART (Includ	ling Autho	r, Title, Date	Pertinent P	ages, Etc.)				
	"A 30-MHz Hy IEEE JOURNA 1385-1394	ybrid Analog/ AL OF SOLII	Digital Clo D-STATE C	ck Recovery ( CIRCUITS, V	Circuit in 2-µ OL. 25, NO.	m CMOS", 1 6, DECEMB	B. Kim BER 19	et al., 90, pp.		
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EXAMINER	-		I	DATE CONS	DERED			,		

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.